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EXAMINER
SOUW, BERNARD E

ART UNIT	PAPER NUMBER
2881	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/583,617	Applicant(s) GORUGANTHU ET AL.	
	Examiner Bernard E Souw	Art Unit 2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *December 05, 2002 (paper # 4/a)*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The Amendment A, filed on 12/05/2002, Paper No.4, in response to the first Office Action dated 08/30/2002 has been entered.

Previous Rejections under 35 USC § 112

2. Applicant's traversal of previous § 112(2) rejections of claims 1, 16 and 20 are not accepted, because Applicant's argument only reiterates Applicant's position, but fails to address Examiner's specific question raised in the 1st Office Action, i.e., whether or not the "*region of the insulator of the SOI structure*" recited in claims 1 (line 4) and 16 (line 4), is the same as that of claim 20 (line2), "*a BOX portion of the SOI structure*". As already stated, the question was raised by the Examiner, because both are insulators, and furthermore, a SOI structure conventionally have insulator layer(s) between the two diffusion regions, one under the gate (=gate insulator layer) and the other a LOCOS layer serving as insulation between the individual transistor units. In this regard, Applicant's definite answer was critically required, in order to conduct a proper examination of claims 1, 16 and 20. However, Applicant has failed to respond properly.

Despite Applicant's refusal to answer Examiner's specific question, a careful inspection of Applicant's figure drawings (Fig.1 showing insulator layer 142 as part of the SOI, and Fig.2 showing BOX layer 250, also part of the SOI) *in comparison* to the prior art drawings (Yoshida, USPAT # 6,137,295), showing in Fig.1 and Fig.5 the layer insulator 1c, has provided the answer sought by the Examiner.

Although Yoshida does not specifically address layer 1c in Fig.1 and Fig.5 as being a BOX layer, it is well known in the art that Yoshida's layer 1c *must* be a BOX layer, which is the same as Applicant's recitation in claim 20. Evidence for this Official Notice can be found in many standard textbooks of semiconductors, and is here provided, e.g., by Belleville et al., Fig.1, and by OKI Technical Review in Figure 1, both showing the same BOX structure as Applicant's, which corresponds to Yoshida's layer 1c. The latter is unambiguously confirmed by the absence of *any other insulator layer* in Yoshida's SOI structure, neither a LOCOS (as in Belleville's and OKI's) nor a gate insulator layer (as in Applicant's layer 142). Note, those two insulator layers might well be inherent in Yoshida's schematics, but were deliberately omitted for being considered irrelevant to Yoshida's invention.

Consequently, the previous § 112(2) rejections of claims 1 and 16 (claim 20 is now cancelled) have been removed by the Examiner by virtue of Belleville's and OKI's, plus a general knowledge in the art, ***despite Applicant's refusal*** to address the § 112(2) rejections based on indefiniteness. As a result, the "*region of the insulator of the SOI structure*" recited in claims 1 and 16, is now interpreted as being *the same* as the "*BOX portion of the SOI structure*" recited in the cancelled claim 20 (line 2). Therefore, the rejection of claims 1 and 16 is now based on Yoshida's Fig.1, which only exposes the BOX, which is essentially different than previously, but is the same as what previously has been applied to the cancelled claim 20.

Applicant is advised that any change of ground of rejection that is solely caused by Applicant's *refusal* to answer (they will be pointed out as such in the following) will not prevent this 2nd Office Action to be made **FINAL**.

Applicant is further advised, that from now on, any attempt to re-interpret the term "*region of the insulator of the SOI structure*" in claims 1 and 16 as being *different* than the term "*BOX portion of the SOI structure*" recited in claim 20, will be subsequently considered as ***New Matter***. Applicant has been given opportunity to give a definite interpretation of these terms in the 1st Office Action. However, Applicant has failed to respond correspondingly. This opportunity will not be made available for a second time. This decision regarding New Matter is a *direct consequence* of Applicant's *refusal* to address the previous § 112(2) rejections, as described above.

Rejections under 35 USC § 102

3. Claims 1-14, 16-19 and 21-23 are rejected under 35 U.S.C. 102(a) and 102(e) as being *anticipated* by Yoshida (USPAT # 6,137,295). The following rejections remain the same as those applied in the 1st Office Action, with the only difference that the applicable SOI device structure, and hence, the associated text recitations, are now referred to Yoshida's Fig.1, instead of previously Fig.5. As stated above, this change of ground of rejection is *solely* necessitated by Applicant's *refusal* to properly respond to Examiner's previous inquiry expressed in the form of § 112(2) rejections of claims 1, 16 and 20. For unambiguity, the claim rejections are reproduced here below, with the changes either underlined or ~~stroked-through~~.

4. Regarding claims 1, 2, 8-11, and 16-19, Yoshida invents a method for analyzing a semiconductor die (2, 3) having silicon-on-insulator (SOI) structure 1s and a back side opposite circuitry 1f & 1g near a circuit side, as shown in Fig.1 (referring to ~~claim 16) and Fig.5 (referring to claims 1 & 2)~~ claims 1, 16 and 20), the method comprising:

- removing substrate 1a shown in ~~Fig.5~~ Fig.1 from the back side of the semiconductor die and exposing a region 1c of the insulator of the SOI structure ~~(the section between the two diffusion regions on the left of the exposed region 1j) where the substrate (1a) has been removed (1j)~~, as recited in ~~Col.6/ll.46-57~~ Col.5/ll.8-13; and
- inducing a detectable response from the exposed region as a function of a portion of the circuitry, as recited in ~~Col.6/ll.51-57~~ Col.5/ll.19-32, and therefrom, analyzing the die, as recited in ~~Col.5/ll.19-32~~ Col.5/ll.52-60.

▶ Regarding claim 2, Yoshida's method of inducing response is by using an electron beam 15 (EB) shown in Fig.2, as recited in Col.5/ll.19-32 & Col.5/ll.53-55.

▶ Regarding claim 8, Yoshida's detectable response is obtained from source/drain region 1e (S/D = diffusion region) shown in Fig.1 ~~and Fig.5~~, as disclosed in Col.5/ll.1-5.

▶ Regarding claim 9, the step of using the BOX layer 1c in Fig.1 ~~and Fig.5~~ as a dielectric in inducing a detectable response, is disclosed in ~~Col.6/ll.51-56~~ Col.5/ll.55-63, i.e., the potential waveform and potential contrast image shown in Fig.3 ~~absence of secondary electrons thereby detected~~.

▶ Regarding claim 10, the step of removing a portion of the substrate 1a to expose a portion of the BOX 1c is shown in Fig.1 and recited in Col.5/ll.8-32.

► Regarding claim 11, Yoshida's method is a post-manufacturing analysis because the device is analyzed after its manufacture is completed, as recited in Col.6/ll.14-19.

► Claims 16 and 17 are apparatus (system) claims reciting limitations that are already rejected in claim 1. The additional recitation of a detector in claim 17 is shown by Yoshida as numeral 14 in Fig.2, as is inherent in Col.5/ll.56-60.

► Regarding claims 18 and 19, the limitation of using a controller to control the substrate removal in claim 17 is rendered obvious by Yoshida's use of the ~~SOI~~ BOX layer as an etching stop to control the substrate removal process, as recited in ~~Col.6/ll.58-60~~ Col.5/ll.33-41, specifically in Col.5/line 39.

► Regarding claim 3, the step of detecting secondary electrons in response to the EB 15 and the portion of the circuitry is recited in Col.5/ll.19-22, whereas the use of a scanning electron microscope (SEM) to generate the electron beam EB is conventional and well known in the art. The latter is an Official Notice supported by many published documents, including Talbot et al. (USPAT #6,091,249) in Col.3/ll.13-16 & Col.6/ll.59-60, as well as by Steffan et al. (USPAT #6,200,823 B1) in Col.1/ll.64-67.

► Regarding claim 4, the step of analyzing the die by detecting the difference between the secondary electron signals obtained from two selected circuit portions is shown by the device 1X in Fig.3, which consists of a plurality of circuit portions (1s & 1f ~~shown in~~ of Fig.1 ~~and Fig.5~~, which represents voltage variations across the plurality of circuit portions, ~~results~~ resulting in a waveform shown in Fig.3, as recited in ~~Col.6/ll.7-11 Col.5/ll.~~ Col.5/ll.53-67.

► Regarding claims 5 and 21, the step of obtaining an image of the die that represents variations in voltage across the plurality of circuit portions is recited in Col.5/ll.57- ~~63~~ 67 and Col.6/ll.1-6, ~~and~~ as shown in Fig.3 and Fig.4.

► Regarding claim 6, the step of using a pulsed EB is disclosed in Col.6/ll.1-6.

► Regarding claim 7, the step of using a coupling power supply and inputting electrical signals to the die to generate a response is inherent in Yoshida's, as implicated by the testing set 11 shown in Fig.2, recited in Col.5/ll.53-60, which inherently and conventionally includes a power supply.

► Regarding claim 12, the electrical stimulus applied to the circuitry in the die is provided by the DUT board 12 shown in Fig.2, recited in Col.5/ll.43-48.

► Regarding claim 13, whether or not to stimulate a response by using the DUT board 12, until a failure is induced in the die, is a mere matter of deliberate choice . As such, the step is unpatentable for only involving routine skill in the art.

► The limitation of claim 14 is inherent in Yoshida's, as shown by the ***continuous*** waveform depicted in Fig.3.

In an alternative § 103(a) rejection, it is ~~basically~~ an automation of a step or method which is normally implemented manually. In this regard, it would have been obvious to one having ordinary skill in the art at the time the invention was made to put the input signals in a continuous loop, since it has been held that broadly providing a mechanical or automatic means to replace manual activity which has accomplished the same result involves only routine skill in the art. *In re Venner*, 120 USPQ 192.

► Regarding claim 22, the limitation that the image of the die shows light and dark areas, the dark areas being indicative of circuit portions having positive voltage greater that that of the lighter areas, is well known in the art, if not even inherent in Yoshida's. This Official Notice is supported by a large number of prior arts, e.g., by Talbot et al. (USPAT #6,091,249) in the Abstract/ll.1-19 and in Col.6/ll.46-48, shown in Fig.3a-d, by Kim et al. (USPAT #2002/0043628A1) in the Abstract/ll.1-6 from bottom.

► Regarding claim 23, the step of using a tester adapter to introduce electrical stimulus to the die is disclosed in testing set 11 shown in Fig.2, as recited Col.5/ll.53-60.

Rejection under 35 USC § 103

5. Claim 15 remains rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al. (USPAT #6,019,249) and Steffan et al. (USPAT #6,200,823 B1). This rejection is 100% the same as that already applied in the 1st Office Action. For the sake of unambiguity, it is reproduced in the following.

Yoshida shows all the limitations of claim 5, as previously applied to the parent claim 1, except the recitation of using a non-defective die as a reference. Talbot et al. disclose a method for analyzing a semiconductor die using an electron beam from a SEM 20 shown in Fig.1, as recited in Col.5/ll.33-57. Talbot's apparatus and method use a defect-free device as reference, as recited in Col.6/ll.65-67.

It would have been obvious to adopt Talbot's use of a non-defective die as a reference in Yoshida's method, since from a single image of a device alone *in the*

absence of other information, it is difficult to determine whether or not the device under testing (DUT) contains an error, as implicated by Talbot et al. in Col.6/ll.63-65.

One would have been motivated to compare the EB image of a DUT with a known, non-defective device, as used by Talbot et al., since a defective die would be much more easily and much more quickly recognized by an operator, especially when the image of the non-defective die is subtracted from the currently measured image of a DUT (die under testing), thus highlighting the defect, as suggested by Steffan et al. in Col.3/ll.8-13.

Response to Applicant's Arguments

6. Applicant's arguments filed 12/05/2002 have been fully considered but they are not persuasive. The following is Examiner's response.

Applicant's arguments against previous rejections of claims 1-19 and 21-23 are moot, because of the new ground of rejection based on Yoshida's Fig.1, instead of on Yoshida's Fig.5.

Final Rejection

7. Applicant's ***refusal*** *to resolve previous § 112(2) rejections* necessitated the new ground(s) of rejection presented in this Office Action. Furthermore, Applicant ***fails*** *to submit any amendment* to overcome the previous rejections and put the claims into a condition of allowance. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP §

706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bernard E Souw whose telephone number is 703 305 0149. The examiner can normally be reached on Monday thru Friday, 9:00 am to 5:00 pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John R Lee can be reached on 703 308 4116. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872 9318 for regular communications and 703 872 9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

bes
December 16, 2002